WHAT IS CLAIMED IS:

1. A method of providing a modulated signal, the method comprising:

providing a phase modulation signal; and

providing amplitude modulation to the phase modulation signal to generate the modulated signal, wherein the phase modulation and amplitude modulation are synchronized.

2. The method of claim 1, wherein the phase modulation and amplitude modulation are synchronized in accordance with a calibration scheme.

3. The method of claim 2, wherein the calibration scheme includes providing the modulated signal having a desired characteristic wherein the phase modulation is reversed when the amplitude modulation is ~~zero.~~ minimum MJ 03/21/01 KJS 3/21/01

4. The method of claim 3, wherein the calibration scheme utilizes a phase jump detector, an envelope detector, and a minimum detector.

5. The method of claim 4, wherein the calibration scheme includes detecting a delay between the phase modulation being reversed and the amplitude modulation being ~~zero.~~ minimum MJ 03/21/01 KJS 3/21/01

6. The method of claim 5, wherein the providing amplitude modulation to the phase modulation signal to generate the modulated signal includes delaying the phase modulation in accordance with the delay.

7. The method of claim 1, wherein the providing amplitude modulation to the phase modulation signal to generate the modulated signal utilizes a gain controlled amplifier.

8. The method of claim 1, wherein the modulated signal is a radio frequency signal.

9. The method of claim 2, wherein the providing a phase modulation signal utilizes a phase lock loop.

10. The method of claim 9, wherein the providing a phase modulation signal utilizes a sigma-delta controlled phase lock loop.

11. A method of modulating first data and second data on a signal, the method comprising steps of:

phase or frequency modulating the signal in accordance with the first data; and

amplitude modulating the signal in accordance with the second data, wherein the steps of phase or frequency modulating and amplitude modulating are coordinated in time with respect to each other to ensure integrity of the first data and the second data.

12. The method of claim 11, wherein a delay circuit is utilized to coordinate in time the phase or frequency modulating step and the amplitude modulating step.

13. The method of claim 12, wherein the delay circuit is calibrated by providing the modulated signal having a desired characteristic, the desired characteristic being when the phase modulation is reversed and the amplitude modulation being simultaneously ~~zero~~ minimum, and detecting a delay between the phase modulation being reversed and the amplitude modulation being ~~zero~~ minimum. mgj 03/21/01 KWS 3/21/01 mgj 03/21/01 KWS 3/21/01

14. A modulator, comprising:

a first data input;

a second data input;

a frequency or phase modulator circuit coupled to the first data input, the frequency or phase modulator circuit providing modulation in response to first data at the first data input; and

an amplitude modulator circuit coupled to the second data input, the amplitude modulator circuit providing modulation in response to second data at the second data input.

15. The modulator of claim 14, further comprising a delay circuit, the delay circuit compensating for time delay for the frequency or phase modulator circuit and the amplitude modulator circuit.

16. The modulator of claim 14, wherein the amplitude modulator is an amplifier.

17. The modulator of claim 16, wherein the second data controls power provided to the amplifier.

18. The modulator of claim 15, wherein the frequency or phase modulator circuit receives an incoming signal and provides a modulated signal to the amplitude modulator circuit.

19. The modulator of claim 18, wherein the delay circuit is coupled between the second input and the amplitude modulator circuit.

20. The modulator of claim 15, further comprising an envelope detector coupled to the amplitude modulator circuit, a minimum detector coupled to the envelope detector, a phase jump detector coupled to the amplitude modulator circuit, and a phase detector/charge pump circuit coupled to the phase jump detector and the minimum detector, the phase detector/charge pump circuit providing a delay signal during calibration of the modulator.